



Hopkins, A., McNeill, N., & Mellor, P. (2016). Drain current injection circuitry for enabling the use of super-junction MOSFETs in a 5kW bidirectional DC-DC converter. In *Proceedings of the 8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016)* <https://doi.org/10.1049/cp.2016.0277>

Peer reviewed version

Link to published version (if available):
[10.1049/cp.2016.0277](https://doi.org/10.1049/cp.2016.0277)

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Drain Current Injection Circuitry for Enabling the Use of Super-Junction MOSFETs in a 5kW Bidirectional DC-DC Converter

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Keywords: Drain current injection, efficiency, super junction, MOSFET, intrinsic diode deactivation

Abstract

The paper assesses the potential of employing super-junction MOSFETs in a high efficiency and low cost bidirectional DC-DC converter for application in electric vehicle systems. Super-junction MOSFETs have a very low conduction loss, however, their poor intrinsic diode recovery behaviour and high output capacitances means that switching losses can be high in voltage source converters. A drain current injection technique is presented that can be used to mitigate the poor switching characteristics and thus realise excellent power conversion efficiencies. Experimental results are given for a circuit operating at 400V, 5kW and 25kHz and the means of achieving a power conversion efficiency >99% is outlined.

1 Introduction

Electric and hybrid vehicles (EV) achieve high overall fuel economy through the use of electrical power to provide flexible management of the on-board energy usage. A range of electrical power conversion units is needed in a typical EV to provide propulsion, recuperate energy and to interface between the on-board energy storage and the energy sources/sinks. If EVs are to be widely adopted these energy conversion units will need to combine excellent efficiency with low cost.

Bidirectional DC-DC power conversion is required, for example in super-capacitor buffer storage systems [1]. Super-junction (SJ) MOSFETs have a very low $R_{DS(on)}$ and reasonable cost making them an attractive alternative to wide-bandgap devices and IGBTs if very high efficiencies are to be attained [2]. However their application in voltage source converters (VSCs) is impeded by the extremely poor reverse recovery behaviour of their intrinsic body drain diode and, furthermore, a highly non-linear output capacitance, C_{oss} . Fig. 1 shows the QV curve for a SJ MOSFET's C_{oss} . (The Engauge Digitiser [3] programme was used to capture this curve from the manufacturer's capacitance graph.) After a freewheeling period, the charge, Q_{rr} , drawn by diode recovery and the charge, Q_{oss} , drawn by the capacitance have to be sourced into a device when the complementary incoming device in a bridge-leg turns on. Adverse effects include high losses in the incoming device and EMI due to the high peak current sourced.

Switching-aid circuitry can be used to address these difficulties whereby C_{oss} is charged from a low-voltage source [4]-[6]. Snubber circuitry has been used in [7], [8]. An auxiliary bridge-leg technique is presented in [9]. Soft switching of SJ MOSFETs may be implemented using the synchronous conducting mode (SCM) [10]. Difficulties with SCM include a high RMS-to-average current ratio in the power devices and chokes, and a load-dependent switching frequency. Another technique is drain current injection (DCI) which has been used with SJ devices at 1kW in [11], and the work in [11] is extended here to a 5kW DC-DC converter also using SJ devices. In this paper, some candidate topologies for the DCI circuit are also reviewed and discussed to inform the selection of a topology to be investigated with a demonstration DC-DC converter.

Future developments in wide-bandgap devices may be appropriate for high power and high-efficiency DC-DC converters. For example, a 60kW converter using SiC MOSFETs is described in [12]. However, silicon devices are likely to continue to be attractive in high volume automotive applications where cost is a paramount consideration.

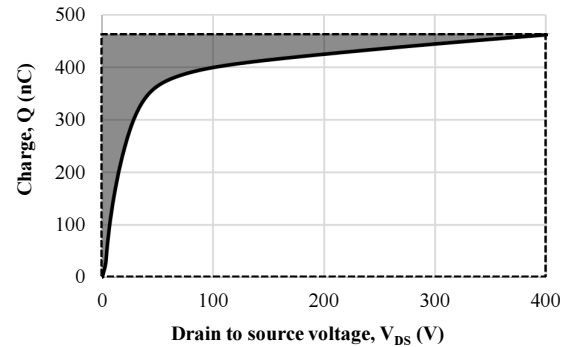


Figure 1: QV characteristic for an Infineon IPW60R041C6 CoolMOS MOSFET.

2 Drain current injection

2.1 Operation of the drain current injection circuit

Fig. 2 outlines the drain current injection (DCI) technique. Here the circuit is operating in the buck converter mode where S2 functions as a synchronous rectifier (SR) and S1 is acting as the control device. For simplicity, only S2 is shown fitted with a DCI circuit. The DCI circuit [11] operates by injecting sufficient current into the drain of a MOSFET operating as a

synchronous rectifier to transiently reverse the net current flowing in it. This deactivates its intrinsic diode and the SR device can then be turned off with minimal consequent recovery charge. However, even if Q_{rr} is obviated, the Q_{oss} drawn by an SJ device is still significant and also has to be addressed. After SR device turn-off, the bulk of Q_{oss} is sourced into C_{oss} by the difference between the injected current and the load current before the incoming, or control, MOSFET (S1 here) switches on. With respect to Fig. 1, if the bulk of Q_{oss} has been supplied, the voltage across the outgoing device, S2, will be at typically 50V and its C_{oss} will have dropped significantly. The incoming device is then turned on without having to source a large transient current.

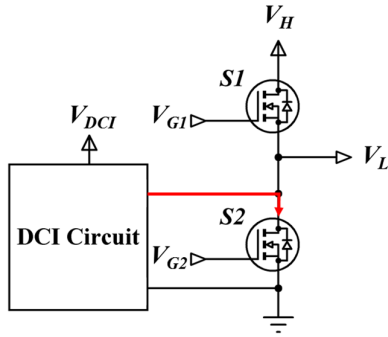


Figure 2: Outline circuit diagram showing bridge leg and the proposed DCI circuitry. The arrow shows the injected SR drain current path.

2.2 Topologies and device selection for the drain current injection circuit

A generic framework DCI circuit is shown in Fig. 3 where an inductor, L , is connected to a high-voltage diode, D . The circuit formed by Q1-4 and D performs the functions of pre-charging L , routing current into the drain of the power MOSFET and allowing transfer of any surplus inductor energy back into the DCI supply rail, V_{DCI} . It is noted that the four locations marked Q1-Q4 can, in principle, be occupied by an open-circuit, diode or active switch (MOSFET) and this gives 3^4 , or 81, possible permutations. Ongoing work is concerned with eliminating impractical permutations and identifying and tabulating the properties of the remainder, based on the work in [13].

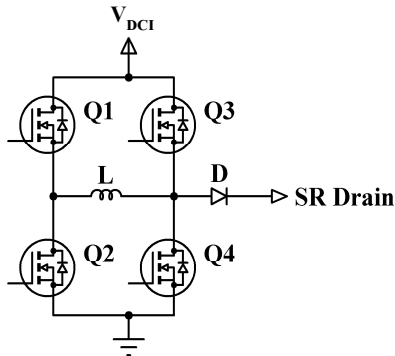


Figure 3: Circuit diagram for the DCI circuit with MOSFETs shown in all four positions Q1-Q4.

The combination of devices may be initially simplified by not considering the use of passive diodes in locations Q1-4, as a MOSFET's functionality always exceeds that of a passive diode. That is, as well as acting as a rectifier, it can act as a controlled switch in the forward direction and as a synchronous rectifier. If only MOSFETs or open-circuits are considered in locations Q1-4, the number of options is reduced to 2^4 , or 16. However, cost is normally lower with a passive diode and complexity is reduced as no control signal is needed. As with resonant gate driver circuits [13], [14] P-channel MOSFETs may be preferred in locations Q1 and Q3 due to the ease of driving their gates.

2.3 Device discussion: Q1

All of the combinations where Q1 is an open-circuit are discarded as this device is required to connect the DCI supply across the inductor. This is reflected in Table 1 where eight options are shown for further consideration. Additionally a diode here cannot establish current in L . A MOSFET is therefore always required in position Q1.

2.4 Device discussion: Q2

Topologies E, F, G and H in Table 1 all have Q2 in place which acts as a return current path from the SR SJ MOSFET's source. This provides a freewheeling path for inductor current when Q1 is switched off. This prevents over-voltages across Q1 and allows recovery of inductor energy. Q2 acts as a synchronous rectifier when a MOSFET is used in this position. However a diode can be used, which would lead to an increase in losses. Without a diode or MOSFET in the Q2 location, it would be necessary to ensure that Q1 is turned off when the inductor current has reached zero, or select a device with an appropriate repetitive avalanche rating.

2.5 Device discussion: Q3, D and Q4

Without Q3 in place, the voltage across Q4 will tend to follow the drain voltage of S2 when current is being injected into S2's C_{oss} and its drain voltage is rising. Q4 would require a high voltage rating, or to be safely rated to have the required repetitive avalanche capability.

Without Q4, a current can still be established in L . However, prior to sufficient current being established to cancel the load current, the current in L will flow through D . This current is not performing any useful task during this phase, as it still has to build up sufficiently and losses are incurred in D .

	Q1	Q2	Q3	Q4
A	1	0	0	0
B	1	0	0	1
C	1	0	1	0
D	1	0	1	1
E	1	1	0	0
F	1	1	0	1
G	1	1	1	0
H	1	1	1	1

Table 1: Device and open-circuit combinations for where a device (either a switch or a diode) is placed in positions Q1-Q4 signified by a '1' or open circuited when '0'.

If Q4 is in place, and has a sufficiently low $R_{DS(on)}$, losses can be mitigated. Whilst, ideally all the current flows in Q4 during the pre-charge phase, if the voltage at the drain of S2 is sufficiently negative during the synchronous rectification stage, D can be brought in to conduction and the potential over L is increased compared to connecting it to 0V via Q4. However, once the full load current has been supported by the DCI circuitry the combined voltage drop over the diode, D, and S2 reduces the rate of charging of L to below that of the case where Q4 is present, if a low $R_{DS(on)}$ device is used. L must be further charged to provide sufficient current to cancel the load current for the injection period and charge the C_{oss} of S2 before S2 can be commutated, thereby preventing conduction of S2's intrinsic body-drain diode. The inductor then discharges via the free-wheeling path. Once the C_{oss} of S2 has been partially charged, the SJ MOSFET S1 can now turn on.

The high voltage diode, D, is the most costly component of the DCI circuitry. However its current rating is directly related to its cost. Its current rating is dependent upon its conduction time. By using a MOSFET in position Q4, to provide a pre-charge current path via Q1-L-Q4, the diode's conduction time is reduced significantly. This allows a more cost effective lower forward current rated device to be used along with a reduction in its losses.

As expected, although the losses in the diode, D, are reduced, losses are incurred in the low voltage MOSFET and Schottky diode, Q3 and Q4. These are due to the two devices conducting during the pre-charge period and some additional losses in Q3 due to the clamping.

3 Experimental circuit

Based on the discussion in Section 2, the circuit outlined in Fig. 4 was implemented for DCI. For experimental purposes, only one power switch was configured with a DCI circuit (S2, as shown in Fig. 2) and the converter was run in the buck mode supplying 4.85kW from a 400V rail into a 200V load at 25kHz. Three TK62J60W SJ MOSFETs in parallel are used to make up each of the power switches in positions S1 and S2. The DCI circuit was operated from a separate 16.4V supply, V_{DCI} .

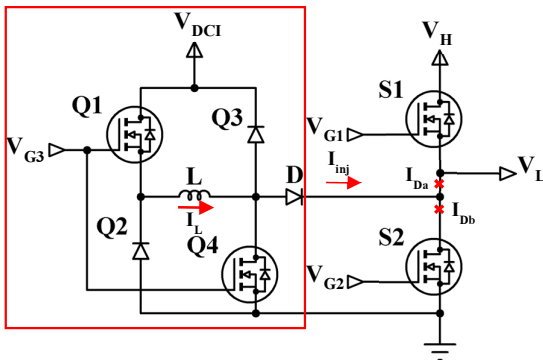


Figure 4: Schematic diagram of a bidirectional DC-DC converter with drain current injection circuitry (enclosed by the red square). The two drain current measurement positions above, I_{Da} , and below, I_{Db} , the injection node (highlighted by the red crosses).

Fig. 5 shows the experimental DCI circuit mounted onto a 5kW bidirectional DC-DC converter. To allow easy comparison, the positions Q1-Q4 may be unoccupied (open-circuit), or occupied with a diode or a MOSFET. The diodes and MOSFETs used for experimentation were in DPAK and PG-TO252-3-11 packages respectively. Given the devices' pin-outs, the PCB can therefore accommodate any of the three scenarios in each position without requiring modification. Only diodes with their cathode connected to the tab of the package were considered.

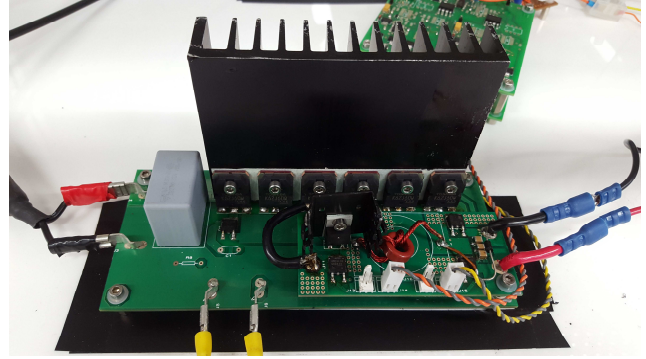


Figure 5: Photograph of the 5kW converter. (S1 and S2 are each composed of three devices in parallel, hence the six discrete devices mounted on the heatsink.)

In the DCI circuit selected, Fig. 4, low voltage MOSFETs are used in positions Q1 and Q4 and Schottky diodes are used in positions Q2 and Q3. Details are:

- D = Rohm SCS220AMC 20A 650V SiC Schottky diode.
- Q1 = Q4 = Infineon IPD90N03S4L-02 30V N-channel MOSFET.
- Q2 = Q3 = STMicroelectronics STPS1045BY 45V Schottky diode.
- L = two turns of 15 strands of 0.315mm diameter copper wire on a T50 -2 Micrometals core.

4 Experimental results

4.1 Initial comparison of circuitry with and without DCI

The circuit in Fig. 5 was run in the normal way without DCI and then with the DCI enabled at a reduced voltage of 50V to allow an initial comparison to be made. A Cree C4D02120A 1.2kV SiC Schottky diode was used in position D1 for this preliminary experiment. This was then replaced with the diode detailed in Section 3 for the full power experimentation. Importantly, a reduced voltage was applied here to avoid circuit failure due to the effects of running without DCI. Results are shown in Fig. 6.

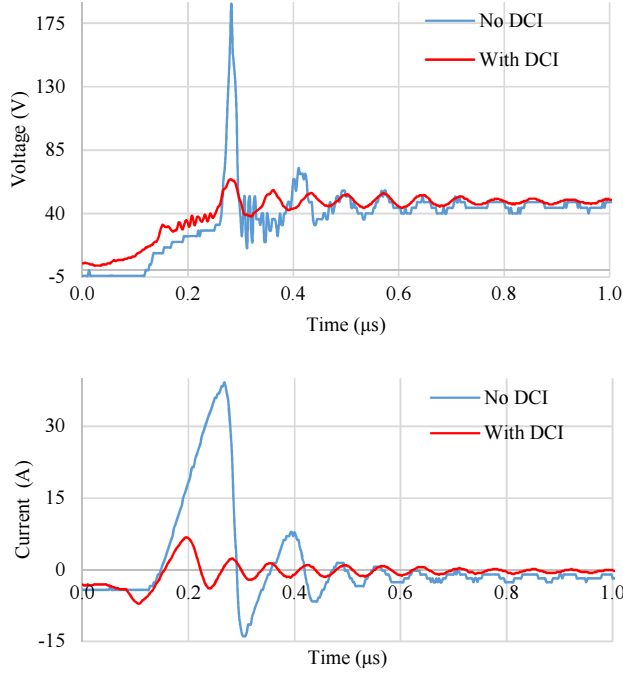


Figure 6 Top: SR device (S2) drain to source voltage (v_{DS}) waveforms for the circuit with (red) and without (blue) the use of DCI. Bottom: SR drain current (I_{DS}) waveforms above injection point (measured with a Hall-effect current probe) for the circuit with (red) and without (blue) the use of DCI. A 50V supply voltage was applied.

4.2 Results at full power

The circuit was then run at close to the full design power (4.85kW) with DCI enabled. Waveforms are shown in Figs. 7 and 8. Thermal photographs are shown in Fig. 9. These results are taken with the circuit in the hard thermal steady-state. It is noted that the converter is run on the flat surface shown in Fig. 5 and that no forced cooling is applied. From the measured power drawn by the DCI circuit and thermal superposition measurements of the main heatsink temperature rise, efficiency is initially estimated at above 99%.

Fig. 8 shows the SR SJ MOSFET drain current measured above, I_{Da} , and below, I_{Db} , the injection node using a Hall-effect current probe and a Rogowski coil respectively. The drain to source voltage (v_{DS}) is also shown. The switching transition and DCI operation can be divided into five distinct stages, highlighted in Fig. 8:

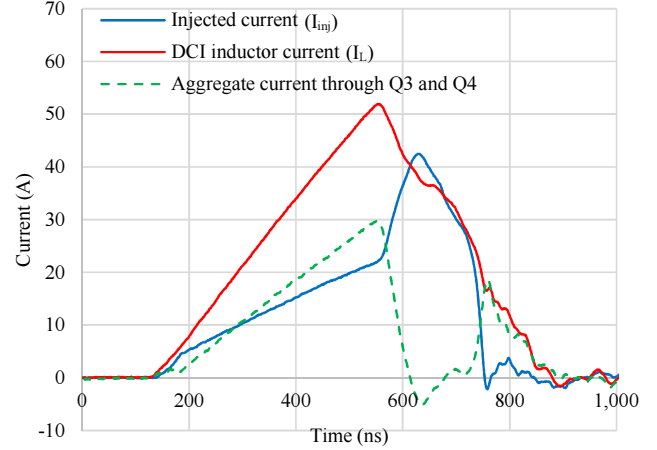


Figure 7: Experimental waveforms obtained from the DCI circuitry of the 4.85kW 400V converter. The DCI inductor current and injected current were measured using a Rogowski coil. The DCI MOSFET's and Schottky diode's current waveforms were obtained by deducting the injected current from the DCI inductor current.

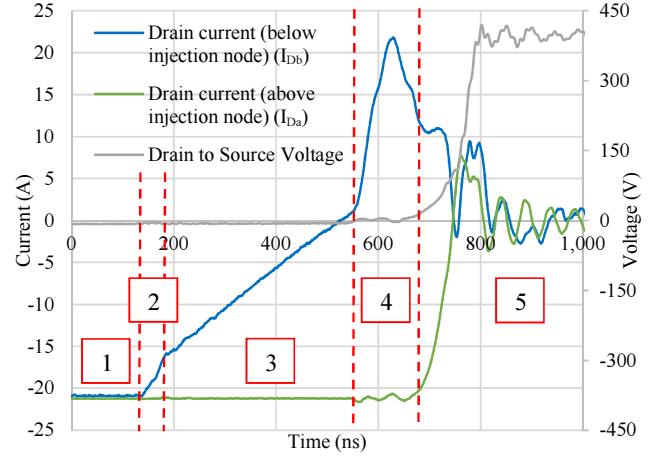


Figure 8: Experimental waveforms obtained from the 4.85kW 400V converter. The drain current waveforms were measured above and below the injection point with a Hall-effect current probe and a Rogowski coil respectively. The five key stages of the switching transition and DCI operation are denoted.

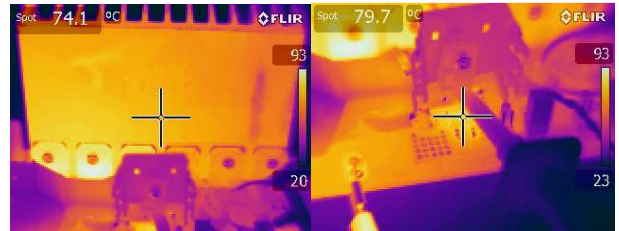


Figure 9: Thermal images of the main heatsink (left) and DCI circuit (right) once thermal equilibrium had been achieved. An ambient temperature of 18°C was measured. A maximum circuit temperature of 93.2°C was recorded on the MOSFETs of S1. A peak temperature of 79.7°C is shown on the thermal image of the MOSFET Q4 in the DCI circuit.

Stage 1: The load current is flowing through the synchronous rectifier SJ MOSFET, S2.

Stage 2: The DCI MOSFET Q1 turns on allowing current to ramp up in the inductor. Q4 has a delayed turn on due to variations in the devices and v_{gs} signals. The current ramps up through the inductor via Q1.

Stage 3: The DCI MOSFET Q4 turns on and a proportion of the inductor charging current flows through this device. With reference to Section 2.5, although it is not intended to inject current into the drain of S2 during this stage, it is seen that the current divides between Q4 and D. This is because the drain of S2 is sufficiently negative with respect to 0V to bring D into conduction. The negative current measured at the drain of the MOSFET (below the injection node, I_{Db}) reduces and the load current is partially supplied by the DCI circuit.

The rate of decrease of the SR SJ MOSFET drain current reduces, however current continues to flow into the SJ MOSFET drain due to the negative voltage observed at this point, caused by the load current and SJ MOSFET's on-state resistance. Again, over the course of this stage, an increasing proportion of the load current is supplied via the DCI circuit. Although there is a slight reduction in the losses of Q4, due to a higher peak current being attained for a shorter pre-charge period, higher losses are experienced in the diode, D.

Stage 4: DCI MOSFETs Q1 and Q4 are switched off. This now injects all of the current which has built up in L into the drain of the SJ MOSFET, S2. The Schottky diode Q2 conducts to complete the circuit. S2 is now turned off as the current in it has now been reversed and its intrinsic diode will therefore not be activated. Turning off S2 allows its C_{oss} to start charging. The voltage at the anode of the D increases but is clamped to the DCI rail voltage by the Schottky diode in position Q3. The current denoted by the dotted line in Fig. 7 flows in Q4, until Q4 turns off at approximately 550ns. Any subsequent flow is in Q3, or Q4 again if the latter avalanches. It is noted that the turn-off of Q1 could be delayed until after that of Q4, but these devices are turned off simultaneously here for simplicity.

Consideration must be made to size the injection diode suitably. Although the injection period is only approximately 200ns, as mentioned, the diode can also conduct during the pre-charge stage. This increase in conduction time leads to an increase in junction temperature. The forward voltage drop characteristics are adversely affected by increasing junction temperatures, especially at high current levels. It is therefore important to select a diode with a suitably high forward current rating. If the diode's forward current rating is insufficient, additional losses are experienced not only in the diode itself but also in the MOSFET Q4. This is caused by the voltage at the drain of Q4 rising above its rated v_{DS} due to a non-ideal clamping action by Q3 and V_{DCI} , allowing Q4 to avalanche. Since the cost of the diode increases with its current and voltage ratings, care must be made to size this component correctly.

The area underneath the drain current (below the injection node, I_{Db}) waveform between approximately 550ns and 750ns in Fig. 8 is around $2\mu C$. It is therefore higher than the anticipated Q_{oss} required to charge the device's C_{oss} up to 90V ($1.2\mu C$). The

difference between these two figures is attributed to the delay of S2 commutating off after the injection phase has started.

Stage 5: S1 turns on during this phase and I_{Da} and I_{Db} are driven to zero. With respect to Fig. 8, it is noted that S1 only supplies a very small charging current of approximately 7-8A peak into S2's output capacitance as the bulk of the required charge has been supplied by the DCI circuit. The injected current then falls to zero as the supply supports the full load current and the device's C_{oss} is charged to approximately 90V. At this point D is reverse biased and stops conducting. Any excess inductor current is forced into Q3 and the associated energy is returned to the supply rail, V_{DCI} . In summary, pre-charging of the SR device's C_{oss} reduces the large and detrimental current transient observed if the C_{oss} has not already been partially charged. This is clearly shown by the SR SJ MOSFET v_{DS} waveform in Fig. 8. The v_{DS} begins to rise at approximately 650ns, which is caused by the charging of the devices C_{oss} from the DCI circuit. As discussed in Section 1, the majority of the Q_{oss} is drawn below 50V. To summarise, the small overshoots of 7-8A observed in the drain current waveforms, I_{Da} and I_{Db} , are caused by the final charging of S2's C_{oss} up to 400V.

4.3 Efficiency estimate at full power

The losses for the main power devices were measured using thermal superposition as discussed in [15]. 25.4W of losses were measured when the converter had reached thermal equilibrium. This does not include gate driver losses, DCI circuit or output inductor losses. The DCI sub-circuit operated from a separate supply. The input power was measured using an oscilloscope with voltage and hall-effect current probes. 5.1W of input power was measured. A small proportion of the power transferred to the DCI circuit will end up on the main power stage heatsink in the process of charging the devices output capacitance. This power has therefore been double counted. Thus the addition of both of these losses gives a pessimistic estimation of the losses in the power stage of the converter at 4.85kW. The efficiency estimate for the converter is therefore 99.4%, excluding gate driver losses and output inductor (choke) losses.

5 Discussion and conclusions

The deployment of super-junction MOSFETs has shown to be feasible in DC-DC converters where forced commutation features in the circuit operation. The potential high levels of switching loss associated with the poor reverse recovery behaviour of the intrinsic diode and large highly non-linear output capacitance of the device are greatly reduced through the use of drain current injection. The technique ensures the drain current is reversed allowing complete diode deactivation and partial C_{oss} charging. No reverse recovery charge is thus required to be sourced from the supply. In conjunction with this, the partial charging of the SJ MOSFET's C_{oss} leads to reduced peak current transients and allows these devices to be implemented in hard switched bridge legs at these higher voltages.

The solution is analogous to the use of auxiliary bridge-legs, is that an arrangement of switches and a reactive component (an inductor) is used to source a current from a suitable voltage without (assuming ideal components) losses. However, apart from the passive diode, D, devices rated at the rail voltage are not required. Apart from avoiding the use of supply-rated devices, additional floating gate drivers are not required and another potential source of shoot-through is not introduced into a VSC.

Although additional circuitry is required when compared with a traditional solution with IGBTs, efficiencies greater than 99% have been shown to be achievable without the need for forced cooling. A gravimetric power density of 12.8kW/kg was achieved here. This power density measurement includes the heatsink but not the choke or gate driver circuits. The largest component of the power stage is the heatsink and its envelope volume was measured to be 208cm³. Further work is likely to include optimisation of the drain current inductor design to reduce losses, investigation of alternative generic DCI circuit frameworks and selection of the high voltage diode. The inductor energy storage requirement will also be addressed.

Acknowledgement

The authors gratefully acknowledge the financial support of the UK Engineering and Physical Sciences Research Council (www.epsrc.ac.uk, Grant No. EP/I031707/1, Vehicle Electrical Systems Integration (VESI)).

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